

- [2] F. U. Rosenberger and C. E. Molnar, "Comments on 'Metastability of CMOS latch/flip-flop,'" this issue, pp. 128-130.
- [3] L.-S. Kim, R. Cline, and R. W. Dutton, "Metastability of CMOS latch/flip-flop," in *Proc. IEEE CICC*, May 1989.

Comments on "Using Cache Mechanisms to Exploit Nonrefreshing DRAM's for On-Chip Memories"

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In [1], an approach to eliminate the need of refreshing for DRAM on-chip caches is presented. Although the authors claim this approach to be new, it had been previously presented in [2].

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Some of the crucial similarities between the mechanism of selective invalidation [1] and the mechanism based on the "row guard circuit" [2] are next sketched:

- A guard circuit for each memory row is presented in [2]. The guard circuit includes two bits (R and V) that behave like bits REFRESH and VALID in [1].
- To update bits R and V , two signals, $U1$ and $U2$, are used in [2]. They behave like the two short pulses, *refresh* and *refresh-1*, proposed in [1].
- Both papers deduce that the refreshing period required for the proposed mechanism must be no longer than one half of the DRAM refreshing period.

We are sorry that neither the authors nor the paper's referees were aware of the mentioned publication.

REFERENCES

- [1] D. D. Lee and R. H. Katz, "Using cache mechanisms to exploit non-refreshing DRAM's for on-chip memories," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 657-661, Apr. 1991.
- [2] J. Cortadella and T. Jové, "Dynamic RAM for on-chip instruction caches," *Comput. Arch. News*, vol. 16, no. 4, pp. 45-50, Sept. 1988.